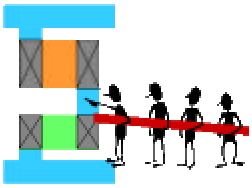
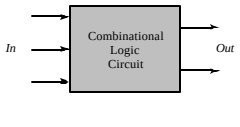
COMBINATIONAL LOGIC



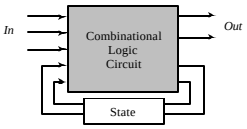
[Adapted from Rabaey's *Digital Integrated Circuits*, ©2002, J. Rabaey et al.]

Combinational vs. Sequential Logic



Combinational

Output = *f(In)*

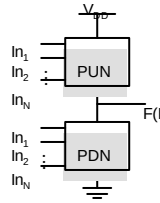


Sequential

Output = *f(In, Previous In)*

Static Complementary CMOS

- Pull-up network (PUN) and pull-down network (PDN)



PMOS transistors only

pull-up: make a connection from V_{DD} to F when $F(In_1,In_2,\ldots In_N) = 1$

pull-down: make a connection from F to GND when $F(In_1,In_2,\ldots In_N) = 0$

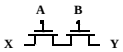
NMOS transistors only

PUN and PDN are dual logic networks

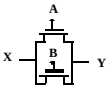
NMOS Transistors in Series / Parallel Connection

Transistors can be thought as a switch controlled by its gate signal

NMOS switch closes when switch control input is high



Y = X if A and B

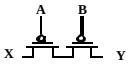


Y = X if A OR B

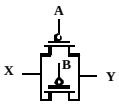
NMOS Transistors pass a "strong" 0 but a "weak" 1

PMOS Transistors in Series / Parallel Connection

PMOS switch closes when switch control input is low



$Y = X$ if $\overline{A}$ AND $\overline{B} = \overline{A + B}$

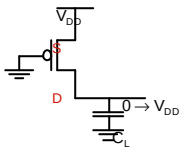


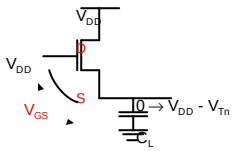
$Y = X$ if $\overline{A}$ OR $\overline{B} = \overline{AB}$

PMOS Transistors pass a "strong" 1 but a "weak" 0

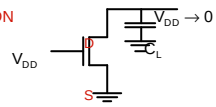
Threshold Drops

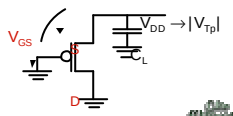
PUN





PDN





Complementary CMOS Logic Style

- PUP is the DUAL of PDN
  (can be shown using DeMorgan's Theorem's)

$$\overline{A+B} = \overline{A}\,\overline{B}$$
$$\overline{AB} = \overline{A}+\overline{B}$$

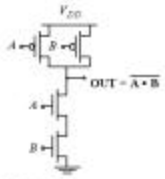
- The complementary gate is inverting

AND = NAND + INV

Example Gate: NAND

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table of a 2 input NAND gate



PDN: G = A B ⇒ Conduction to GND

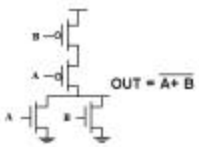
PUN: F = $\overline{A}$ + $\overline{B}$ = $\overline{AB}$ ⇒ Conduction to V_{DD}

$\overline{G(In_1, In_2, In_3, \ldots)} = F(\overline{In_1}, \overline{In_2}, \overline{In_3}, \ldots)$

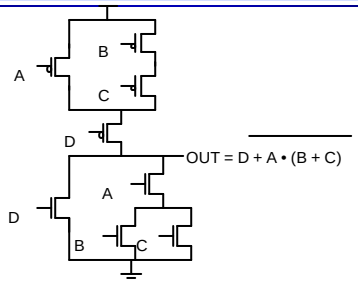
Example Gate: NOR

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

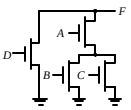
Truth Table of a 2 input NOR gate



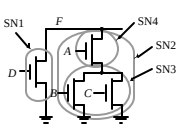
Complex CMOS Gate



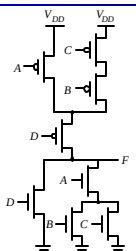
Constructing a Complex Gate



(a) pull-down network



(b) Deriving the pull-up network hierarchically by identifying sub-nets

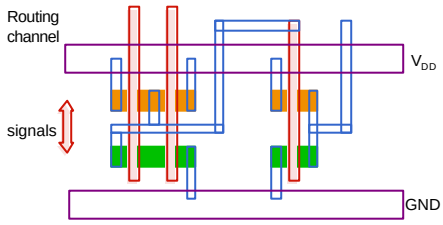


(c) complete gat

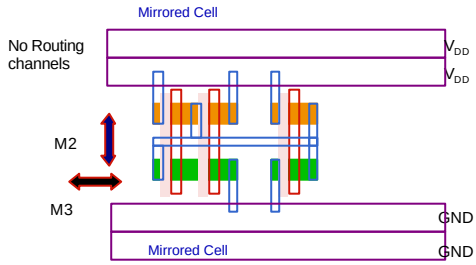
Cell Design

- Standard Cells
  - » General purpose logic
  - » Can be synthesized
  - » Same height, varying width
- Datapath Cells
  - » For regular, structured designs (arithmetic)
  - » Includes some wiring in the cell
  - » Fixed height and width

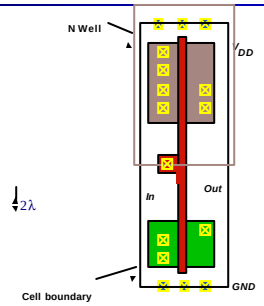
Standard Cell Layout Methodology – 1980s



Standard Cell Layout Methodology – 1990s



Standard Cells



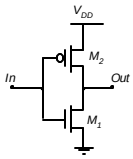
Cell height 12 metal tracks
Metal track is approx. 3λ + 3λ
Pitch =
repetitive distance between objects

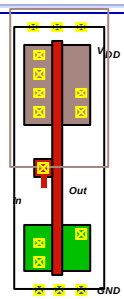
Cell height is "12 pitch"

Rails ~10λ

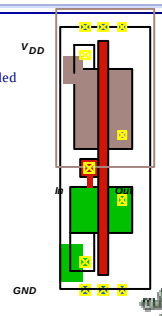
Standard Cells

With minimal diffusion routing

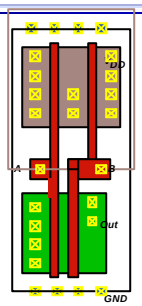




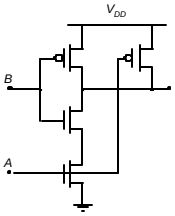
With silicided diffusion



Standard Cells



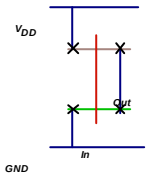
2-input NAND gate



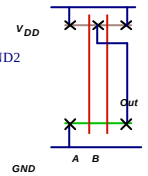
Stick Diagrams

Contains no dimensions
Represents relative positions of transistors

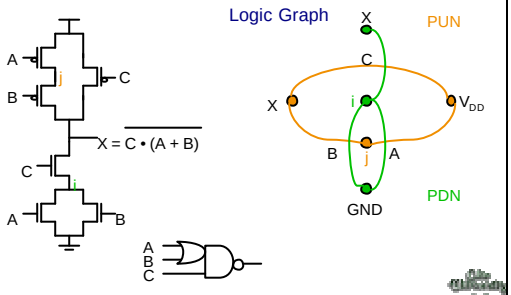
Inverter



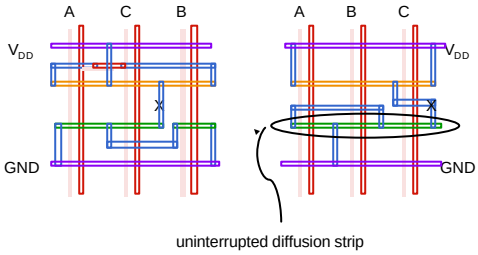
NAND2



Stick Diagrams

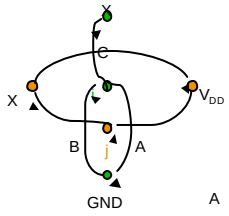


Two Versions of C • (A + B)

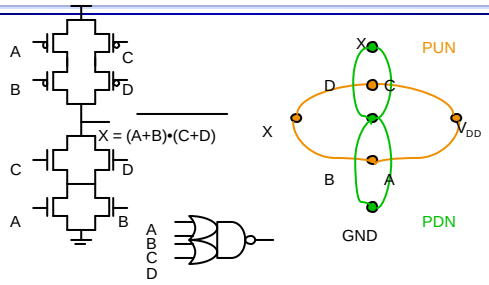


Consistent Euler Path

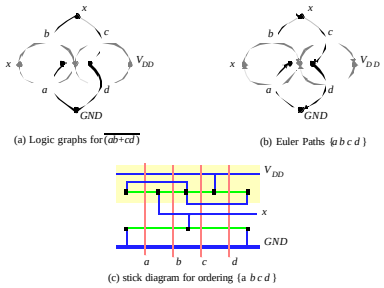
- An uninterrupted diffusion strip is possible only if there exists a Euler path in the logic graph
  - Euler path: a path through all nodes in the graph such that each edge is visited once and only once.



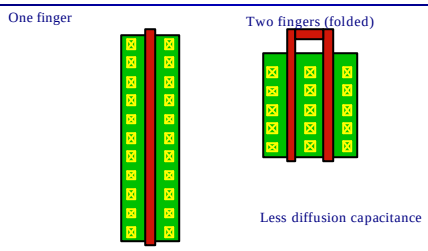
OAI22 Logic Graph



Example: x = ab+cd



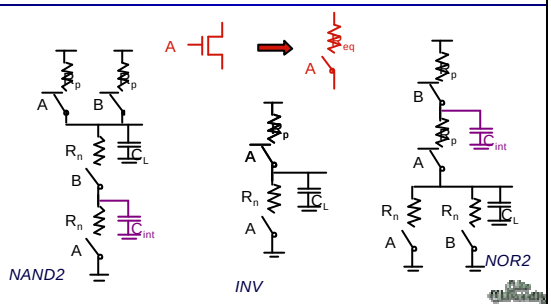
Multi-Fingered Transistors



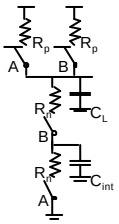
CMOS Circuit Styles

- Static complementary CMOS - except during switching, output connected to either V_{DD} or GND via a low-resistance path
  - » high noise margins
    - – full rail to rail swing
    - – V_{OH} and V_{OL} are at V_{DD} and GND, respectively
  - » low output impedance, high input impedance
  - » no steady state path between V_{DD} and GND (no static power consumption)
  - » delay a function of load capacitance and transistor resistance
  - » comparable rise and fall times

Switch Delay Model

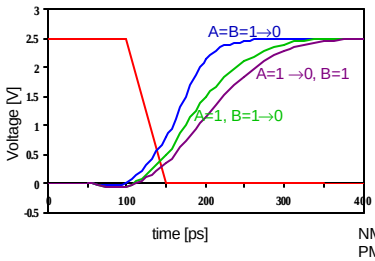


Input Pattern Effects on Delay



- Delay is dependent on the pattern of inputs
- Low to high transition
  - » both inputs go low
    - – delay is 0.69 R_p/2 C_L
  - » one input goes low
    - – delay is 0.69 R_p C_L
- High to low transition
  - » both inputs go high
    - – delay is 0.69 2R_n C_L

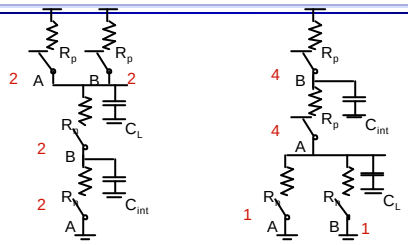
Delay Dependence on Input Patterns



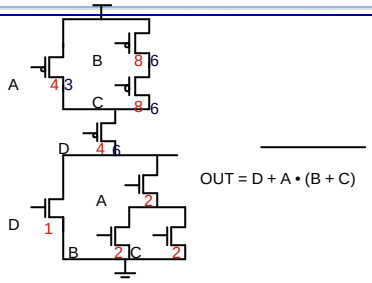
Input Data Pattern	Delay (psec)
A=B=0→1	67
A=1, B=0→1	64
A= 0→1, B=1	61
A=B=1→0	45
A=1, B=1→0	80
A= 1→0, B=1	81

NMOS = 0.5µm/0.25 µm
PMOS = 0.75µm/0.25 µm
C_L = 100 fF

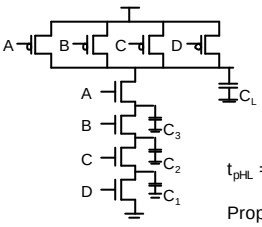
Transistor Sizing



Transistor Sizing a Complex CMOS Gate



Fan-In Considerations

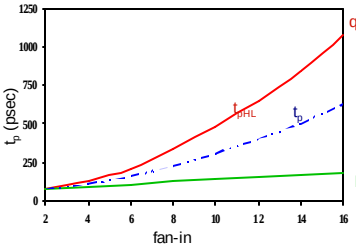


Distributed RC model (Elmore delay)

$t_{pHL} = 0.69\ R_{eqn}(C_1+2C_2+3C_3+4C_L)$

Propagation delay deteriorates rapidly as a function of fan-in – quadratically in the worst case.

t_p as a Function of Fan-In

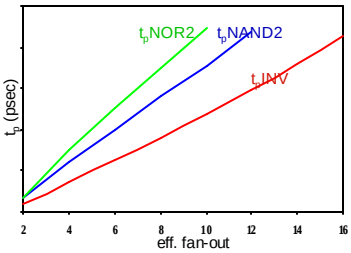


quadratic

Gates with a fan-in greater than 4 should be avoided.

linear

t_p as a Function of Fan-Out



All gates have the same drive current.

Slope is a function of "driving strength"

Problems with Complementary CMOS

- Gate with N inputs requires 2N transistors
  - other circuit styles use N+1 transistors
- t_p deteriorates with high *fan-in*
  - increases total capacitance
  - series connected transistors slows down gate
- *fan-out* loads down gate
  - 1 fan-out = 2 gate capacitors (PMOS and NMOS)

$$t_p = a_1 FI + a_2 FI^2 + a_3 FO$$